



Current Mode PWM Controller

Description

GP3201 is a monolithic current mode PWM control IC designed for high performance low standby current off line flyback power converter applications. To meet the latest ENERGY STAR external power supply efficiency requirement at light and no load conditions, Green Mode Control circuits integrated to improve the power efficiency and without audible noise. Slope compensation is integrated to ensure the stability at heavy loading. Current Sense signal process by Leading Edge Blanking circuit prevents the false trigger when drive external MOSFET. Soft switching control and frequency jitter technique designed to drive the gate reduce the EMI noise. The Gate-drive output is clamped at 18V to protect the power MOS.

GP3201 Built-in with protection functions including Cycle-by-Cycle current limiting, over load protection (OLP) and under voltage lockout (UVLO).

GP3201 offer SOT23-6, SO-8 and DIP8 packages.

Features

- Green mode Control
- Low Startup / Operating Current
- No-audible-noise
- Frequency jitter function to reduce EMI noise
- Programmable PWM Switching Frequency
- Internal Slope Compensation
- Leading Edge Blanking
- Gate Max Output Voltage Clamp at 18V
- Overload Protection (OLP).
- Over Current Protection (OCP)
- Under Voltage Lockout (UVLO)

Applications

Offline AC / DC flyback converter for

- **Battery Charger**
- **Power Adaptor**
- **Set-Top Box Power Supplies**
- **Open-frame SMPS**
- **PC 5V Standby Power**

Pin Assignments

SOT-26 Package

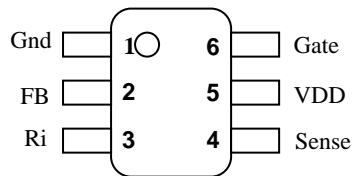
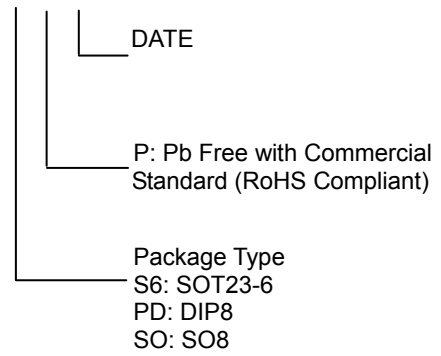


Fig. 1. Pin Assignment of GP3201 for SOT-26

Ordering Information

GP3201□□□



SO8 and DIP8 Package

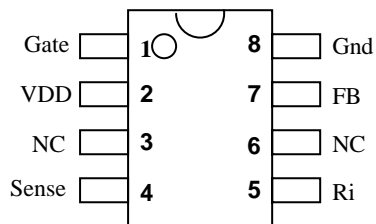


Fig. 2. Pin Assignment of GP3201 for SOP8 and DIP8

Typical Application Circuit

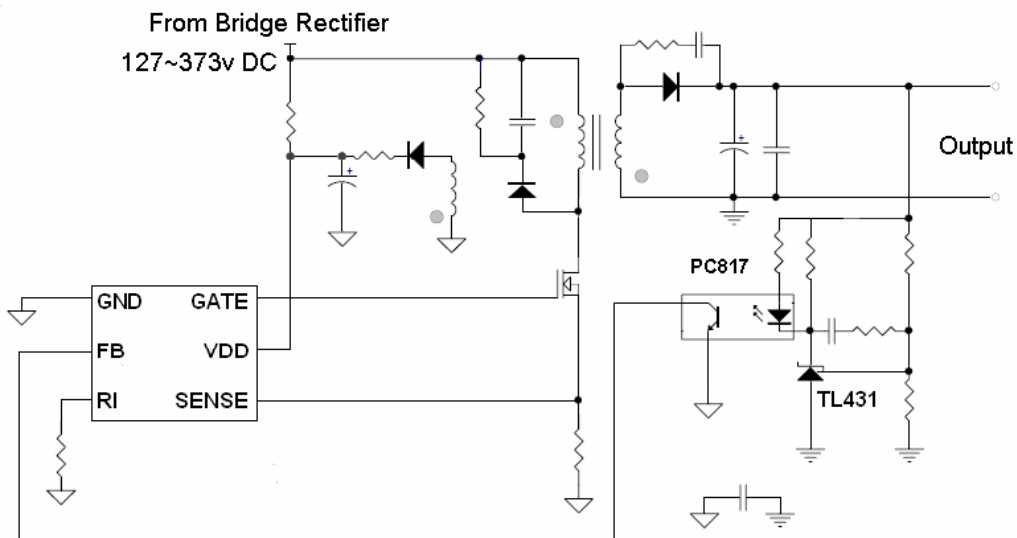


Figure3. Typical Application Circuit of GP3201

Functional Pin Description

| Pin # | Pin Name | Pin Function |
|-------|----------|---|
| 1 | GND | Ground |
| 2 | FB | The PWM duty cycle is determined by voltage level into this pin and the current-sense signal from Photo couple. |
| 3 | RI | A resistor connected between OSC and GND sets the PWM frequency. |
| 4 | SENSE | Current sense input pin. Connected to MOSFET current sensing resistor node. |
| 5 | VDD | Power Supply input pin. |
| 6 | GATE | Drive to the power MOSFET Gate. |

Block Diagram

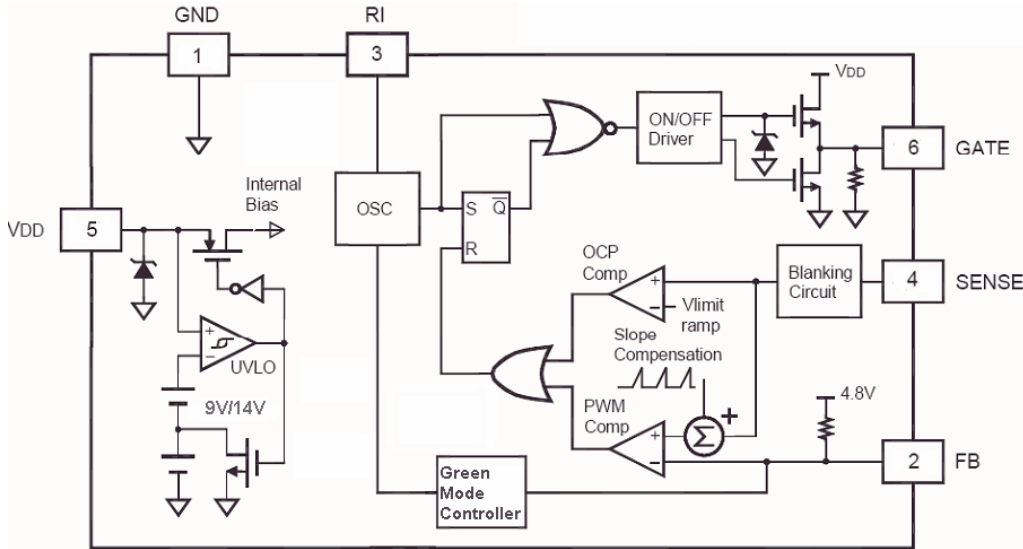


Figure 4. Block Diagram of GP3201

Absolute Maximum Ratings

- VDD to GND----- - 0.3V to + 30V
- VDD clamped current----- 10mA
- VFB, VSENSE and VOsc to GND----- - 0.3V to + 6V
- Junction Temperature----- - 20°C to + 150°C
- Storage Temperature Range----- - 55°C to + 160°C

Note : Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

Recommended Operating Conditions

- Supply Voltage, VDD----- 25V
- Osc resistor value----- 91kOhm
- Operation Temperature Range----- - 20°C to + 85°C

Electrical Characteristics

(TA = 25°C, R_{osc} = 91kOhm, VDD=16V, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|------------------------|---|------|------|------|-------|
| SUPPLY SECTION | | | | | | |
| Chip start up current via VDD pin | I _{set} | Vdd=12V, measure current into VDD pin | | 10 | 30 | uA |
| Operation current | I _{op} | VDD=16V,VFB=3V | | 1.4 | | mA |
| VDD UVLO enter | UVLO_L | | 8 | 9 | 10 | V |
| VDD UVLO exit | UVLO_H | | 13 | 14 | 15 | V |
| VDD clamp voltage | VDD_CLP | I(VDD)=10mA | | 34 | | V |
| FEEDBACK SECTION | | | | | | |
| PWM input gain | A_PWM | ΔVFB / ΔVCS | | 2 | | |
| VFB open loop voltage | VFB_O | | | 5.3 | | V |
| FB pin short circuit current | VFB_S | Short FB pin to Gnd and measure current | | 0.8 | | mA |
| Zero duty cycle FB threshold | VFB_th_L | | | 0.75 | | V |
| Power limiting FB threshold | VFB_th_P | | | 3.7 | | V |
| Power limiting delay time | T_PL_D | | | 35 | | mS |
| Input impedance | R_FB | | | 6 | | KΩ |
| Maxim duty cycle | D_MAX | VDD=18V, FB=3V, CS=0 | | 75 | | % |
| OSCILLATOR | | | | | | |
| Normal oscillation frequency | F _{osc} | | 60 | 65 | 70 | KHz |
| Frequency temperature stability | Δf_Temp | TA -20°C to +100°C | | 5 | | % |
| Frequency supply stability | Δf_Sup | VDD 12-25V | | 5 | | % |
| Operating R _{osc} range | R _{osc_range} | | 50 | 91 | 150 | KΩ |
| R _{osc} open load voltage | R _{osc_open} | | | 2 | | V |
| Burst mode base frequency | F _{osc-BM} | | | 22 | | KHz |
| Frequency modulate range (jitter) | Δf_osc | | -3 | | 3 | % |
| Jitter frequency | f_jitter | | | 32 | | Hz |
| CURRENT SENSE SECTION | | | | | | |
| Leading Edge Blanking time | T _{blank} | | | 300 | | nS |
| Sense pin input impedance | R _{sense} | | | 40 | | kΩ |
| Over current threshold voltage at Sense pin | VTH_OC | FB=3.3V | 0.70 | 0.75 | 0.80 | V |
| Over current protect delay | T _{OC_D} | CS > VTH_OC, FB=3.3V | | 75 | | nS |
| GATE OUTPUT | | | | | | |
| Output low level | VOL | I _o = -20mA | | | 0.8 | V |
| Output high level | VOH | I _o = 20mA | 10V | | | V |
| Output voltage clamped level | VG_CLP | | | 18 | | V |
| Output rising time | T _r | Load = 1nf | | 220 | | nS |
| Output falling time | T _f | Load = 1nf | | 70 | | nS |

Operation Description

The GP3201 includes all necessary function to build an easy use and cost effective solution for low power supplies to meet the latest international power conservation requirements.

Start-up current

A very low level startup current was designed so that VDD could be charged up above UVLO threshold level and quick starts up achieved. A large value startup resistor used to minimize the power loss.

Green Mode Operation

At light load or no load condition, the switch loss become the major loss of the power supply, to reduce the power wasted in light and no load condition, a voltage controlled oscillator designed to achieve Green Mode operation of the power supply. The controller sensing the load condition from the voltage of FB pin. In light load condition, the FB voltage will decrease, when VFB is lower than a chip internal set threshold voltage, the oscillator frequency will decrease proportion to the FB voltage and reduce the power supply operating frequency. The minimum frequency is set around 23kHz. When loading further reduced, the VFB decrease further, the power supply will operate in power saving mode to increase the efficiency at no load condition. No audible noise in any load condition.

Oscillator Operation

A resistor connect from Osc pin to ground generate a constant current source of GP3201. This current charge / discharge an internal capacitor to control the internal clock and determine switching frequency.

Increase the resistance will decrease the current source and reduce the switching frequency. The formula for Rosc and switching frequency is set as below:

$$f_{PWM} = 6000 / R_{osc} \text{ (kHz)}$$

Built-in Slope Compensation

The voltage across the sense resistor is sensed for PWM control and Pulse by Pulse current limit. Built-in slope compensation circuit adds a voltage ramp onto the current sense input voltage. It improves the close loop stability and prevents the sub-harmonic oscillation of current mode PWM control scheme.

Leading Edge Blanking

Each operation cycle when the power MOSFET switch on, a turn-on spike may sensed from the sense-resistor. To avoid premature termination of the switching pulse, a 270 nsec leading-edge blanking time is built in. Conventional RC filtering can therefore be reduced. During this blanking period, the current-limit comparator is disabled and it cannot switch off the gate driver.

Gate Driver

The output stage of GP3201 is a fast totem pole gate driver. Cross over conduction has been avoided to minimize heat dissipation, increases efficiency and enhances reliability. The output driver is clamped by an internal 18V Zener diode in order to protect power MOSFET transistors against undesirable gate over voltage. A soft driving waveform is implemented to minimize EMI.

Frequency Jitter

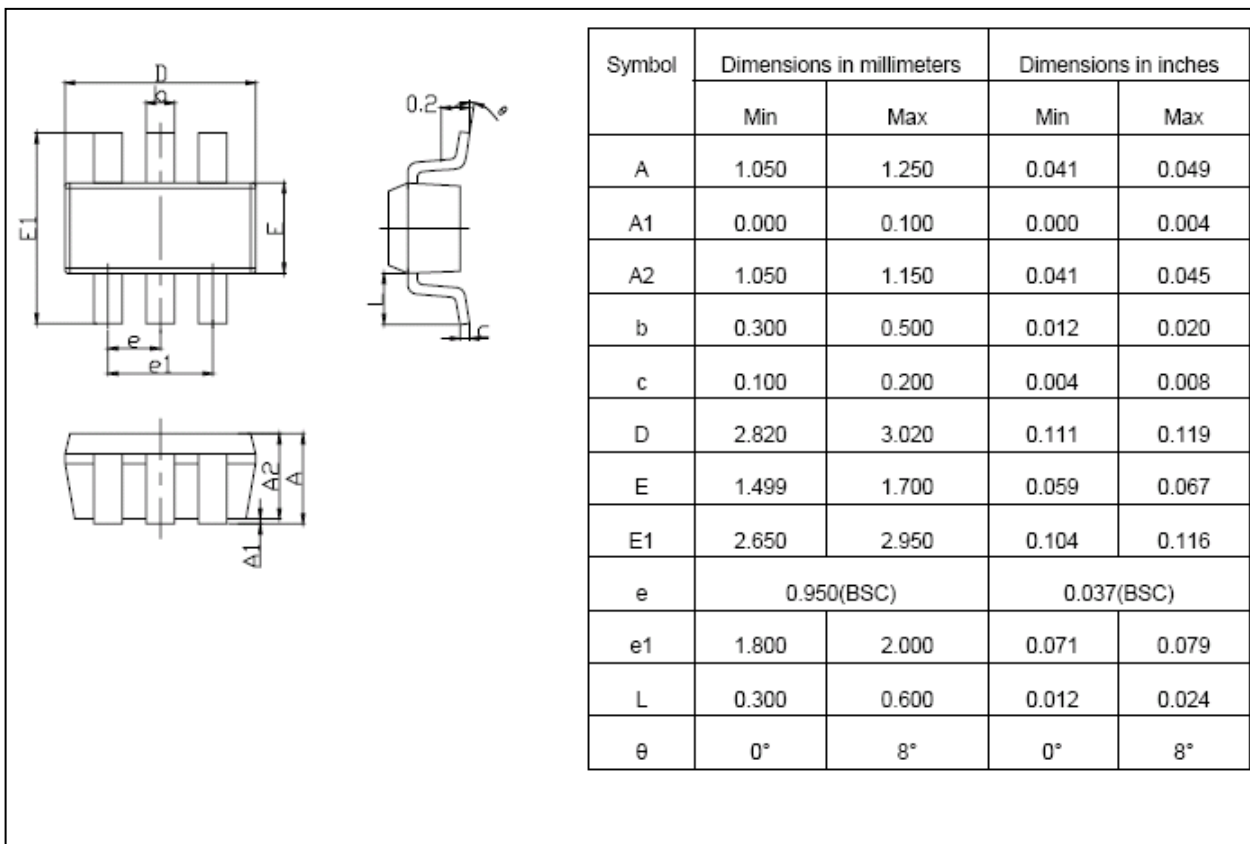
The frequency jitter function is integrated in the controller, the jitter is modulated by a periodic ramp signal, the modulate signal frequency is much larger than the oscillator frequency, By implementing this control method, the EMI noise has a wider spectrum but with lower amplitudes as well as its energy.

Protect Functions

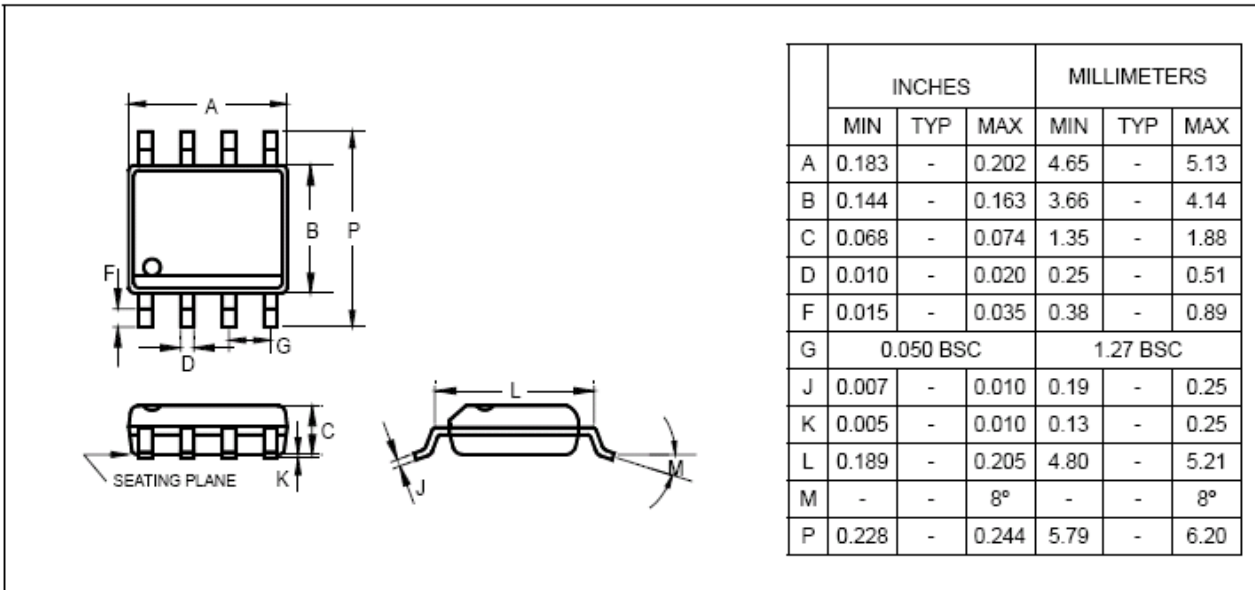
To increase the reliability of power supply system many protection functions is integrated in this controller, including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP) and over voltage clamp, Under Voltage Lockout on VDD (UVLO). At overload condition when FB input voltage exceeds

power limit threshold value for more than TD_PL (power limit debounce time), the controller reacts to shut down the output power MOSFET. Device restarts when VDD voltage drops below UVLO limit. VDD is supplied by transformer auxiliary winding output. It is clamped when VDD is higher than threshold value. The power MOSFET is shut down when VDD drops below UVLO limit and device enters power on start-up sequence thereafter.

SOT23-6 DIMENSION



8-Pin Plastic SO



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